We claim:

1. A method for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

defining a plurality of grooves into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer;

mounting said wafer to a flat rigid substrate to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate;

mechanically removing a predetermined portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining of mounted to said substrate; and

releasing said plurality of dies from said substrate.

2. The method of claim 1 further comprising disposing a planarizing layer of low stress material on said front surface of said wafer into which said plurality of grooves have been defined prior to mounting said front surface of said wafer to said flat substrate.

3. The method of claim 1 further comprising disposing a layer of low stress material on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

4. The method of claim 1 where mounting said flat substrate to said front surface of said wafer comprises affixing an optically flat substrate to said front surface of said wafer.

5. The method of claim 4 where affixing said optically flat substrate comprises affixing said front surface of said wafer to a surface of said substrate which has vertical variations of approximately one micron or less across said surface.

6. The method of claim 1 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to mounting to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when mechanically removing a portion of said wafer.

7. The method of claim 1 wherein defining said plurality of said grooves in said wafer comprises defining grooves approximately 50 microns deep into said front surface of said wafer.

8. The method of claim 7 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of 50 microns or less.

9. The method of claim 8 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of approximately 25 microns or less.

10. The method of claim 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of a low viscosity low stress adhesive.

11. The method of claim 10 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to affixing to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when said grooves are mechanically formed in said wafer.

12. The method of claim 11 where releasing said plurality of dies comprises disposing said thinned backside surface of said wafer onto a pin block and dissolving said adhesive layer, thereby leaving said plurality of separated dies on said pin block.

13. The method of claim 1 further comprising mounting said dies onto a flexible film.

14. The method of claim 13 further comprising sealing said die mounted on said flexible film.

15. The method of claim 13 where mounting said die on said flexible film further comprises electrically coupling said integrated circuit in said die to metalizations provided on said film.

16. The method of claim 15 where electrically coupling said integrated circuit on said die to metalizations on said film comprises disposing said die with said front surface in contact with said metalizations on said film and coupled thereto by means of conductive epoxy.

17. The method of claim 1 where mounting said wafer to said substrate comprises affixing said front surface of said wafer to substrate on a surface of said substrate provided with a plurality of grooves defined in said substrate to facilitate the flow of material across said surface of said substrate between said surface of said substrate and said front surface of said wafer.

18. The method of claim 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using low viscosity, low stress materials disposed between said front surface and said flat substrate.

19. The method of claim 18 further comprising pressing said wafer and substrate together with said low viscosity and low stress material therebetween

and curing said material while maintaining said pressure between said wafer and substrate.

20. The method of claim 1 where mechanically removing said wafer comprises grinding said backside portion of said wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell.

21. The method of claim 20 where grinding with a least one advance rate and dwell comprises at least one reduction in said advance rate.

22. The method of claim 21 further comprising polishing said thinned backside surface of said wafer by a dry chemical etch having an etch rate of less than one micron per minute or a mechanical polish having an advance rate of less than one micron per minute.

23. The method of claim 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

24. The method of claim 1 further comprising stacking a plurality of separated dies prepared by said method, and electrically interconnecting said dies.

25. An assembly used for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

a plurality of grooves defined into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said front surface a predetermined distance which is less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; and

a flat rigid substrate mounted to said wafer to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate and to expose said backside of said wafer for partial mechanical removal of said backside by an amount sufficient to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining of mounted to said substrate.

26. The assembly of claim 25 further comprising a low viscosity, low stress layer disposed between said front surface of said wafer and said substrate to affix said front surface of said wafer to said substrate.

27. The assembly of claim 26 wherein said low viscosity, low stress layer includes a polyimide layer disposed on said front surface.

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